

INTEGRATED STRUCTURE OF INDUCTANCES WITH SHARED VALUES ON A  
SEMICONDUCTOR SUBSTRATE

BACKGROUND OF THE INVENTION

5    Field of Invention

The present invention relates to inductances with shared values formed on a semiconductor substrate, and especially to such inductances intended for operating in a range of frequencies greater than several hundreds of MHz, which will be here called the RF range.

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Description of the Related Art

Fig. 1 schematically shows a perspective view of an inductance L integrated on a semiconductor substrate 1, intended for operating in the RF range. Inductance L includes a substantially planar conductive track 2 deposited on a first insulating layer 5 of the semiconductor substrate. Conductive track 2 forms a winding comprised of a succession of rectilinear segments arranged between a first end 3, on the external side of the winding, and a second end 4, on the internal side of the winding. The rectilinear segments forming the winding are substantially parallel two by two and separated by a constant distance. A first terminal A of inductance L is formed by end 3 of track 2. A second terminal B of inductance L is connected to end 4 of track 2 via a conductive segment 6 passing under the segments of track 2.

Fig. 2 schematically shows a circuit 8 for receiving RF signals using integrated inductances. Circuit 8 includes a first processing chain T1 enabling reception of signals modulated on a carrier of frequency f1, for example, on the order of 900 MHz, and a second processing chain T2 enabling reception of signals modulated on a carrier of frequency f2, for example on the order of 1800 MHz. Such a circuit is useable in a device like a cell phone provided for operating either only with frequency f1, or only with frequency f2, or indifferently with one of frequencies f1 or f2.

Circuit 8 includes an input 10 connected to an antenna 12. The first processing chain T1 includes a low-noise amplifier 14, a mixer 16, and a first local oscillator (not shown). Amplifier 14, provided for amplifying signals modulated on a carrier of frequency  $f_1$ , is connected to input 10 and provides a differential signal to mixer 16. Mixer 16 further receives a sinusoidal signal of frequency  $f_{11}$  provided by the first local oscillator. It provides a signal of intermediary frequency  $IF = f_1 - f_{11}$  to an output 18. The second processing chain T2 includes a low-noise amplifier 20, a mixer 22, and a second local oscillator (not shown). Amplifier 20, provided to amplify signals modulated on a carrier of frequency  $f_2$ , is connected to input 10 and provides a differential signal to mixer 22. Circuit 22 also receives a sinusoidal signal of frequency  $f_{12}$  generated by the second local oscillator and provides a signal of intermediary frequency  $IF = f_2 - f_{12}$  to output 18, the intermediary frequencies provided by mixers 16 and 22 being the same. A control means (not shown) activates one of the processing chains according to the desired frequency.

Mixer 16 includes a so-called “Gilbert cell” (not shown), having terminals G1 and G2 respectively connected to the first terminals A1, A2 of two inductances L1 and L2. The second terminals B1 and B2 of inductances L1 and L2 are connected to the circuit ground. Inductances L1 and L2 have equal values. When the Gilbert cell operates, the alternating currents flowing through inductances L1 and L2 have the same frequency, the same absolute value, and opposite directions. The value of inductances L1 and L2 is inversely proportional to the operating frequency.

Similarly, mixer 22 includes a Gilbert cell (not shown) having two terminals G3 and G4 respectively connected to the first terminals A3, A4 of two inductances L3 and L4. The second terminals B3, B4 of inductances L3 and L4 are connected to the circuit ground. Inductances L3 and L4 have equal values. Frequency  $f_2$  being greater than frequency  $f_1$ , inductances L3 and L4 have a value smaller than that of inductances L1, L2.

In an implementation in integrated form of circuit 8, the four inductances L1, L2, and L3, L4 occupy a significant surface area, which increases the cost of the integrated circuit.

## SUMMARY OF THE INVENTION

An embodiment of the present invention provides an inductance structure occupying a reduced surface on a semiconductor substrate.

- Another embodiment of the present invention provides an integrated circuit
- 5 including a structure of inductances on a semiconductor substrate, intended for operating at frequencies greater than several hundreds of MHz, including a first inductance formed by a conductive track and having first and second terminals respectively connected to each of the two ends of the conductive track, including a second inductance formed by the conductive track between the second terminal and any intermediary point of the conductive
- 10 track connected to a third terminal, said second and third terminals forming the two terminals of the second inductance, and means for setting the third terminal to high impedance when the first inductance is used.

According to an embodiment of the present invention, the conductive track is formed of rectilinear segments.

- 15 According to an embodiment of the present invention, the conductive track is substantially of octagonal shape.

According to an embodiment of the present invention, said intermediary point is connected to the third terminal via a rectilinear conductive segment.

- 20 According to an embodiment of the present invention, said conductive segment is substantially perpendicular to the conductive track.

- According to an embodiment of the present invention, the circuit includes at least one second inductance structure symmetrical to the first structure and formed of the same elements, in which the conductive tracks of the first and second structures are interleaved so that the two conductive tracks have the same length, and in which the 25 distances from each of the intermediary points of each of the conductive tracks of the first and second inductance structures to the second end of said conductive tracks are equal.

According to an embodiment of the present invention, the circuit includes first and second processing chains, the first chain including a first mixer adapted to using a first frequency and the second chain including a second mixer adapted to using a second

frequency, the first terminal of the first inductance being connected to the first mixer, the second terminal of the first inductance being connected to a circuit ground, and the third terminal of the second inductance being connected to the second mixer.

According to an embodiment of the present invention, the circuit includes a  
5 second inductance structure identical to the first structure, the first terminal of the first inductance of the second structure being connected to the first mixer, the second terminal of the first inductance of the second structure being connected to the circuit ground, and the third terminal of the second inductance of the second structure being connected to the second mixer.

10 The foregoing objects, features and advantages of the present invention, will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1, previously described, shows a perspective view of a conventional  
15 inductance;

Fig. 2, previously described, schematically shows a circuit using several inductances;

Fig. 3 schematically shows a top view of an inductance structure according of the present invention;

20 Fig. 4 schematically shows a circuit using the inductance structure according to the present invention;

Fig. 5 schematically shows a top view of a first alternative of the present invention; and

25 Fig. 6 schematically shows a top view of a second alternative of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

Only those elements likely to ease the understanding of the present invention have been shown. Same references refer to same elements in the different drawings.

5 An embodiment of the present invention provides forming an integrated circuit including an inductance structure comprised of a first inductance formed of a conductive track, and of a second inductance formed between one end of the conductive track and any point of the conductive track, connected to a terminal by a connection conductive segment. Thus, a bi-band circuit like circuit 8 can use either the first  
10 inductance or the second inductance according to its operating mode.

Such an inductance structure implies the connection of a conductive segment to any intermediary point of the first inductance. Now, those skilled in the art have a strong prejudice following which the connection of such a conductive segment creates insuperable problems. Especially, those skilled in the art of the field of RF frequencies would think that a conductive segment connected to any point of the first inductance would increase the stray capacitance of the track forming the first inductance in a manner which would be difficult to quantify. Now, an increase in the stray capacitance of an inductance decreases the resonance frequency of a circuit incorporating this inductance. Further, those skilled in the art consider that the presence of an intermediary connection point causes an electromagnetic coupling due to the modified parasitic elements between the conductive segment and the conductive track, likely to modify the values of the inductances in a manner which is difficult to quantify.  
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A contribution of the present inventors has been to perform tests and to notice that the modification of the resonance frequencies of the first and second inductances by the unused conductive track segments is actually negligible if the first and second inductances are not simultaneously used, and if the ends of the unused track segments, and at least that of the conductive segment connected to the intermediary point, are maintained at high impedance.  
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Fig. 3 schematically shows a top view of an inductance structure L5, L6 according to an embodiment of the present invention. Inductance L5 includes a conductive track 38 forming a winding comprised of a succession of rectilinear segments between a first end 40, on the external side of the winding, and a second end 42, on the internal side 5 of the winding. A first terminal A5 of inductance L5 is formed by the first end 40 of track 38. A second terminal B5 of inductance L5 is connected to the second end of track 38 via a first conductive segment 44. An inductance L6 is formed by the portion of conductive layer 38 located between end 42 and a predetermined point J of track 38. A second conductive segment 46 enables connecting point J to a first terminal A6 of inductance L6. 10 Preferably, conductive segment 46 is substantially perpendicular to the segments of track 38. The second terminal of inductance L6 is formed by terminal B5.

The applicant has acknowledged that, even in the RF range, the coupling existing between conductive segment 46 and track 38 has a negligible influence upon the value of inductance L5 when terminal A6 is maintained at high impedance.

15 Inductance structure L5, L6 substantially occupies the same surface as inductance L5 alone, which represents a considerable surface area gain. This structure applies to any circuit using a single one of the two inductances L5, L6 at a time during which the terminal of the unused inductance can be maintained at high impedance.

20 Fig. 4 illustrates a bi-band circuit similar to that of Fig. 2, in which same references designate same elements.

Two inductance structures L7, L8 on the one hand, and L9, L10 on the other hand, replace inductances L1, L3, and L2, L4 of the circuit of Fig. 2. Terminal G1 of mixer 16 is connected to the first terminal, A7, of inductance L7. The second terminal, B7, of inductance L7 is grounded. Terminal G3 of mixer 22 is connected to the first terminal, 25 A8, of inductance L8. Similarly, terminal G2 of mixer 16 is connected to the first terminal, A9, of inductance L9. The second terminal of inductance L9 is grounded. Terminal G4 of mixer 22 is connected to the first terminal, A10, of inductance L10.

When the first processing chain T1 is used, mixer 16 is activated and mixer 22 is deactivated. Inductances L7 and L9 are then used. Terminals G3, G4 of mixer 22,

which is deactivated, are at high impedance. Similarly, when the second processing chain T2 is used, mixer 22 is activated and mixer 16 is deactivated. Inductances L8 and L10 are used. Terminals G1, G2 of mixer 16, which is deactivated, then are at high impedance.

The surface area occupied by inductance structures L7, L8, and L9, L10  
5 according to the present invention is substantially half the surface area occupied by  
inductances L1, L2, L3, and L4.

Fig. 5 schematically shows a top view of a device including two structures  
of two inductances according to the present invention, respectively L11, L12, and L13,  
L14, which are symmetrical and interleaved. The first inductance L11 includes a  
10 conductive track 50 formed of a succession of rectilinear segments arranged in a winding  
between a first end 52, on the external side of the winding, and a second end 54, on the  
internal side of the winding. The first terminal A11 of inductance L11 is formed by end 52  
of track 50. The second terminal B11 of inductance L11 is connected to end 54 of track 50  
via a conductive segment 56.

15 Inductance L12 is formed by the portion of conductive track 50 located  
between end 54 and a predetermined point J1 of track 50. A conductive segment 58  
enables connecting point J1 to a first terminal A12 of inductance L12. The second terminal  
of inductance L12 is formed of terminal B11.

Inductance L13 includes a conductive track 60 formed of a succession of  
20 rectilinear segments arranged according to a symmetrical winding with respect to the  
winding of conductive track 50. The segments of track 60 cross the segments of track 50 in  
several points, by a contactless overlapping. Tracks 50, 60 have the same length and  
inductances L11 and L13 have the same value. Track 60 includes a first end 62, on the  
external side of the winding, and a second end formed by the second end 54 of track 50.  
25 The first terminal A13 of inductance L13 is formed by end 62 of track 60. The second  
terminal of inductance L13 is common with the second terminal B11 of inductance L11.

Inductance L14 is formed by the portion of conductive track 60 located  
between end 54 and a predetermined point J2 of track 60. A conductive segment 64

enables connecting point J2 to a first terminal A14 of inductance L14. The second terminal of inductance L14 is formed by terminal B11.

Such an arrangement of tracks 50 and 60 can be used in the circuit of Fig. 2. Thus, the two inductances L11, L13 can be used to replace inductances L1 and L2 while 5 the two inductances L12 and L14 may be used to replace inductances L3 and L4. Further, the proximity of terminals A11 and A13 eases the connection of inductance pair L11 and L13 respectively to terminals G1 and G2 of mixer 16 by tracks of same length and same impedance. Similarly, the proximity of terminals A12 and A14 eases the connection of inductance pair L12 and L14 respectively to terminals G3 and G4 of mixer 22.

10 Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. Thus, the use of an inductance structure according to the present invention in a bi-band receive circuit such as the circuit of Fig. 4 has been described. Of course, the inductance structure according to the present invention can be used in a bi-band transmit circuit and, generally, 15 in any circuit comprised of two inductances used non-simultaneously.

Further, although, for clarity, inductances according to the present invention having a winding with a substantially square or rectangular shape have been shown in Figs. 3 and 5, those skilled in the art will easily adapt the present invention to inductances having a winding with any shape.

20 As an example, Fig. 6 shows an inductance structure L15, L16 according to the present invention, the conductive track 70 of which has a substantially octagonal shape between a first end 72, on the external side of the winding, and a second end 74, on the internal side of the winding. A first terminal A15 of inductance L15 is formed by first end 72 of track 70. A second terminal B15 of inductance L15 is connected to second end 74 of 25 track 70 via a conductive segment 76. Inductance L16 is formed by the portion of conductive track 70 located between end 74 and a point J3. A second conductive segment 78 enables connecting point J3 to a first terminal A16 of inductance L16. The second terminal of inductance L16 is formed by terminal B15.

In the foregoing description, the second inductance of the inductance structures according to the present invention is formed by the portion of the conductive track located between the second terminal of the first inductance and a predetermined point. However, those skilled in the art will easily adapt the present invention to the case  
5 where the second inductance is formed by the portion of the conductive layer located between the first terminal and said predetermined point.

Only inductance structures according to the present invention using one conductive track and including two inductances have been described, the second inductance being formed between a predetermined point of the conductive track and one  
10 end of the conductive track. The prejudice discarding the possibility of branching a conductive segment at any point of the conductive track having been overcome, it is believed that it is possible to adapt the present invention to a structure comprised of three inductances or more, each inductance being formed between a specific predetermined point of the conductive track and one end of the conductive track.

15 Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

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